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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/668,385 | 09/23/2003 | M. Kelly Lalonde | CA920020048US1 | 2493 |

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| EXAMINER |
|---|
| ROSSOSHEK, YELENA |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/668,385 | LALONDE ET AL. | |
| | Examiner | Art Unit | |
| | Helen Rossoshek | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4,6-17,19-29,31-33,35,37,40-44 and 49-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-17,19-29,31-33,35,37,40-44 and 49-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to the Application 10/668,385 filed 09/23/2003 and amendment filed 04/18/2006.

2. Claims 1-4, 6-17, 19-29, 31-33, 35, 37, 40-44, 49-53 remain pending in the Application. Claims 5, 18, 30, 34, 36, 38, 39, 45-48 have been cancelled from the Application.

3. Applicant's arguments have been fully considered and are persuasive.

### *Claim Objections*

4. Claims 32, 37, 49, 53 are objected to because of the following informalities: claims have improper dependency, for example, claim 37 depends from cancelled claim 36.

Claim 49 line 7 after "identifier" delete "ot" insert –of--

Appropriate correction is required.

### *Claim Rejections - 35 USC § 101*

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-4, 6-17 are rejected under 35 U.S.C. 101 because the claimed invention is not supported by either a claim or Specification asserted utility or a well established utility. The claimed invention lacks patentable utility. Having a statement "A software system . . ." in the preamble leads to the conclusion that an apparatus/machine will be described by claim, instead it comes to limiting a software code/program, which is a product. But in order to claim a proper product, the following has to be claimed: a

storage in the media of a computer system and it must to be executed to implement particular steps to achieve desired results, such as steps if method design of the integrated circuit, for example. Therefore claim 1 misses all mentioned steps to disclose a system/software program, so it lacks a utility of the software system.

7. Claims 1-4, 6-17 are also rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported by either a claims or Specification asserted utility or a well established utility for the reasons set forth above, one skilled in the art clearly would not know how to use the claimed invention.

***Claim Rejections - 35 USC § 112***

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 19-25 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: since claim 19 states in the preamble "A software system", it is expected to have steps of article manufacture, i.e. **components/devices to perform** steps of the method, instead claim 19 contains limitations describing **steps of the method,** therefore essential omitted elements are elements/components of the system.

***Claim Rejections - 35 USC § 102***

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-4, 6-17, 19-29, 31-33, 35, 37, 40-44, 49-53 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishikawa (US Patent 6,122,443).

With respect to claims 1, 19 and 26 Nishikawa teaches a software system for constrained graphs within an apparatus and method for arrangement and moving of an objects and wires of the integrated circuit layout (abstract; col. 1, ll.14-17; ll.56-58), which is realized by computer system including software program/application (col. 32, ll.4-23), comprising software code for implementing a graph, the graph being constructed using a plurality of subgraphs having each a pre-defined grouping of a plurality of graphical elements circuit layout is represented by constraint graph having plurality of subgraphs as shown on the Fig. 4 (col. 2, ll. 10-14) and Fig. 5 representing a portion of the circuit layout/constraint graph as a subgraph including a group of objects and wires (graphical elements) (col. 4, ll.55-57), wherein all objects having predetermined positional relationship (col. 6, ll.28-29); software code for repositioning elements of a subgraph as shown on the Figs. 47 and 50, wherein object/graphical element C removed from one subgraph and repositioned into other subgraph (col. 27, ll.57-58); and software code for repositioning other subgraphs when the other subgraphs are affected by the repositioning of the elements of the subgraph by moving a new subgraph (tree K) to the right side to obtain a new layout (col. 27, ll.67; col. 28, ll.1-2).

With respect to claim 43 Nishikawa teaches a layout manager defined by a layout manager interface, the layout manager interface provided by a software system for use

in the design of software applications in which a constrained graph is displayed to a user within an apparatus and method for arrangement and moving of an objects and wires of the integrated circuit layout (abstract; col. 1, ll.14-17; ll.56-58), which is realized by computer system including software program/application (col. 32, ll.4-23), wherein modified circuit layout by compactor being displayed as a constraint graph and/or portion of constraint graph representing the portion of the circuit layout (col. 7, ll.34-40; col. 19, ll.48-51), the layout manager comprising: a first layout manager class, wherein the first layout manager class is extended to define one or more second layout manager classes, wherein an instance of each of the one or more second layout manager classes represents a layout manager, wherein each of the one or more second layout manager classes implements a method within performing the process of modification of the circuit layout repeatedly to obtain different potions of the circuit layout/constrained graph modifying the layout displaying to the user the difference between the layout before change and that after change (col. 19, ll.42-53); identifying a plurality of subgraphs in the graph within circuit layout, which is represented by constraint graph having plurality of subgraphs shown on the Fig. 4 (col. 2, ll. 10-14); receiving an identifier of an input subgraph in the graph within ability of the apparatus to specify objects and wires (subgraphs) in the graph of the circuit layout (col. 6, ll.32-35); determining from the identifier a selected subgraph to be shifted (col. 6, ll.4-7); commanding a repositioning and display of the graphical elements of the selected subgraph by calling the method implemented by the second subgraph class of which the selected subgraph is in instance (col. 19, ll.42-53) by moving the subgraph C to the

right in a horizontal direction as shown on the Fig. 60 (col. 29, ll.57-59); determining other subgraphs affected by the repositioning of the graphical elements of the selected subgraph by showing the subgraph C, which was moved to the right in a horizontal direction, subgraphs D and C became to close to each other (subgraph D is affected by repositioning of the subgraph C); commanding a repositioning and display of the affected subgraphs within performing shifting subgraph D, which will be moved to increase a distance between D and C in vertical direction (col. 29, ll.61-67; col. 30, ll.1-3).

With respect to claim 44 Nishikawa teaches a method of displaying a constrained graph, the constrained graph being constructed by a plurality of subgraphs having each a predefined grouping of subgraphs having each a predefined grouping of a plurality of graphical elements within apparatus and method for arrangement and moving of an objects and wires of the integrated circuit layout (abstract; col. 1, ll.14-17), wherein circuit layout is represented by constraint graph having plurality of subgraphs shown on the Fig. 4 (col. 2, ll. 10-14) and Fig. 5 representing a portion of the circuit layout/constraint graph as a subgraph including a group of objects and wires (graphical elements) (col. 4, ll.55-57), wherein the apparatus is enabled to display constraint graph and/or portion of constraint graph representing the portion of the circuit layout (col. 7, ll.34-40; col. 19, ll.48-51), receiving from a user an input for deleting at least one graphical element from or adding at least one graphical element to a particular subgraph within specifying the portion of the layout to be changed by input by user (col. 7, ll.34-40); determining whether to reposition one or more graphical elements from the

predefined grouping of the graphical element of the particular subgraph in response to the addition or deletion of the at least one graphical element (col. 6, ll.4-7); repositioning one or more graphical elements of the particular subgraph if it is determined that the one or more graphical elements from the predefined grouping of the graphical elements are to be repositioned by moving the subgraph C to the right in a horizontal direction as shown on the Fig. 60 (col. 29, ll.57-59); determining whether location of one or more subgraphs is affected by the repositioning of the one or more graphical elements of the particular subgraph by showing the subgraph C, which was moved to the right in a horizontal direction, subgraphs D and C became to close to each other (subgraph D is affected by repositioning of the subgraph C); repositioning, if one or more subgraphs are affected, the one or more affected subgraphs within performing shifting subgraph D, which will be moved to increase a distance between D and C in vertical direction (col. 29, ll.61-67; col. 30, ll.1-3) within user's instruction to complete or repeat performance of moving elements or subgraphs (col. 19, ll.54-57).

With respect to claim 49 Nishikawa teaches a method of displaying a constrained graph, said graph comprising a plurality of graphical elements and a plurality of subgraphs, wherein each of said plurality of subgraphs comprises a grouping of said graphical elements within apparatus and method for arrangement and moving of an objects and wires of the integrated circuit layout (abstract; col. 1, ll.14-17), wherein circuit layout is represented by constraint graph having plurality of subgraphs shown on the Fig. 4 (col. 2, ll. 10-14) and Fig. 5 representing a portion of the circuit layout/constraint graph as a subgraph including a group of objects and wires (graphical

elements) (col. 4, ll.55-57), wherein the apparatus is enabled to display constraint graph and/or portion of constraint graph representing the portion of the circuit layout (col. 7, ll.34-40; col. 19, ll.48-51), the method comprising: determining from an identifier of an input subgraph in said graph, a selected subgraph to be repositioned within ability of the apparatus to specify objects and wires (subgraphs) in the graph of the circuit layout (col. 6, ll.32-35); and repositioning the graphical elements of said selected subgraph as shown on the Fig. 38, wherein the portion of the circuit layout represented by constraint graph including subgraph which groups plurality of graphical elements, such as A, B and C (col. 24, ll.9-11), wherein this subgraph is moved to the right as a group of components (col. 24, ll.13-16).

With respect to claim 50 Nishikawa teaches a method for of displaying a constrained graph, said graph comprising a plurality of graphical elements and a plurality of subgraphs, wherein each of said plurality of subgraphs comprises a grouping of one or more of said graphical elements within apparatus and method for arrangement and moving of an objects and wires of the integrated circuit layout (abstract; col. 1, ll.14-17), wherein circuit layout is represented by constraint graph having plurality of subgraphs shown on the Fig. 4 (col. 2, ll. 10-14) and Fig. 5 representing a portion of the circuit layout/constraint graph as a subgraph including a group of objects and wires (graphical elements) (col. 4, ll.55-57), wherein the apparatus is enabled to display constraint graph and/or portion of constraint graph representing the portion of the circuit layout (col. 7, ll.34-40; col. 19, ll.48-51), said method comprising: repositioning the graphical elements of a subgraph within said graph as shown on the Fig. 38, wherein

the portion of the circuit layout represented by constraint graph including subgraph which groups plurality of graphical elements, such as A, B and C (col. 24, ll.9-11), wherein this subgraph is moved to the right as a group of components (col. 24, ll.13-16); and initiate a repositioning of the graphical elements of subgraphs affected by said repositioning of the graphical elements of said subgraph as shown on the Figs. 58 and 60 by another example representing constraint graphs for the portion of circuit layout (col. 29, ll.41-43) the subgraph C was moved to the right side in a horizontal direction as shown on the Fig. 60 subgraphs D and C became to close to each other (subgraph D is affected by repositioning of the subgraph C), wherein subgraph D will be moved to increase a distance between D and C in vertical direction (col. 29, ll.61-67; col. 30, ll.1-3).

With respect to claims 2-4, 6-17, 20-25, 27-29, 31-33, 35, 37, 40-42, 51-53 Nishikawa teaches:

Claims 2, 27, 51: further comprising software code for displaying the graphical elements of each subgraph in a specified layout format as shown on the Fig. 4 (col. 2, ll. 10-14) and Fig. 5 representing a portion of the circuit layout/constraint graph as a subgraph including a group of objects and wires (graphical elements) (col. 4, ll.55-57), wherein all objects having predetermined positional relationship (col. 6, ll.28-29);

Claims 3, 28, 40: wherein said specified layout format comprises a layout selected from the following group: a horizontal layout and a vertical layout within circuit layout having horizontal and vertical directions (col. 1, ll.46-50);

Claims 4, 29, 41: wherein said specified layout comprises a directional layout (col. 1, ll.52-56);

Claims 6, 21, 31: wherein said first subgraph class comprises an abstract class by positioning the objects in the constraint graph and weighting their connectivity (col. 4, ll.43-50);

Claims 7, 32, 52: further comprising: a layout manager adapted to: initiate the repositioning and display of the graphical elements of a plurality of subgraphs in said graph by commanding the repositioning and display of the graphical elements of a selected subgraph in said graph (col. 19, ll.42-53);

Claims 8, 20, 22, 33, 53: wherein said layout manager is further adapted to: identify a plurality of subgraphs in said graph within circuit layout, which is represented by constraint graph having plurality of subgraphs shown on the Fig. 4 (col. 2, ll. 10-14); receive an identifier of an input subgraph in said graph (col. 7, ll.60-63); determine from said identifier a selected subgraph to be shifted (col. 6, ll.4-7); and command said selected subgraph to reposition and display the graphical elements (col. 19, ll.42-53);

Claim 9: further comprising a first layout manager class which can be extended to define one or more second layout manager classes within repeatedly performing modification of the circuit layout by commanding by user or system (col. 19, ll.42-47; ll.54-57); and wherein said layout manager comprises an instance of a second layout manager class within completion determining section 104 shown on the Fig. 10 as one of the steps in performance to modify circuit layout (col. 19, ll.31-40; 58-61);

Claims 10, 35: wherein the selected subgraph determined from said identifier comprises said input subgraph within ability of the apparatus to specify objects and wires (subgraphs) in the graph of the circuit layout (col. 6, ll.32-35);

Claims 11, 23: wherein said instance of a second layout manager class is created when one or more graphical elements are added to or deleted from said graph as shown on the Figs. 47 and 50, wherein object/graphical element C removed from one subgraph and repositioned into other subgraph (col. 27, ll.57-58), wherein Fig. 50 represents a second layout manager class (i.e. modified layout);

Claims 12, 24, 37: further comprising a module for obtaining input from a user, wherein a request to add or delete graphical elements from said graph is generated from said input within specifying the portion of the layout to be changed by input by user (col. 7, ll.34-40);

Claims 13, 25: wherein data associated with subgraphs identified by an instance of said second layout manager class is stored in a map, and wherein said map is used by instances of said second subgraph classes in determining affected subgraphs by creating table shown on the Fig. 14, which is used for storing the information of location each object in subgraph of constraint graph (col.14, ll.66-67; col. 15, ll.1-11);

Claim 14: wherein said map comprises a hash map within the table shown on the Fog. 14;

Claim 15: wherein said repositioning of the graphical elements of said specific subgraph requires that said graphical elements be shifted either horizontally or vertically in said graph within repositioning and display of the affected subgraphs within

performing shifting subgraph D, which will be moved to increase a distance between D and C in vertical direction (col. 29, ll.61-67; col. 30, ll.1-3), and by moving the subgraph C to the right in a horizontal direction as shown on the Fig. 60 (col. 29, ll.57-59);

Claim 16: wherein said specified layout comprises a directional layout within circuit layout having horizontal and vertical directions (col. 1, ll.46-50);

Claims 17, 42: wherein a subgraph comprises a further subgraph within structuring the constraint graph ad plurality of subgraphs, wherein each subgraph might represent single object/comportment or group of the objects/components as shown for example on the Fig. 38 (col. 24, ll.21-24).

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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